REMARKS

Claims 24-26 have been added. Thus, claims 1-26 are pending in the application. Reconsideration of the application in light of the following remarks is respectfully requested.

I. REJECTION OF CLAIMS 1-20 UNDER 35 U.S.C. § 103

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,270,265, Hemmenway et al, hereinafter referred to as Hemmenway in view of U.S. Patent No. 6,159,844, Bothra, hereinafter referred to as Bothra. Reconsideration and withdrawal of this rejection is respectfully requested for at least the following reasons.

i. Hemmenway does not teach plasma etching of a hard mask.

Claims 1-20 recite *plasma etching* to strip the sacrificial material *and the hard mask*, which Hemmenway and Bothra, alone or in combination, fail to teach. The Office Action contends that Hemmenway teaches plasma etching the sacrificial material and the hard mask and points to a citation (Column 4, lines 14-17) as justification, but this assertion is incorrect. The reference only discloses alternate methods of removing the *buffer material overlying the hard mask* (Column 4, line 15). Thus, the alternate methods are limited to only the buffer material overlying the hard mask and *not* buffer material in the gaps nor the hard mask layer, itself. Hemmenway only teaches removal of the hard mask by a *wet oxide etch* (Column 3, lines 61-64), which can damage underlying silicon as pointed out in Applicants' specification (*see* page 7, lines 27-30) instead of the plasma etch recited in claims 1-20.

ii. Hemmenway does not teach plasma etching sacrificial material completely from the gaps.

Claim 8 recites plasma etching sacrificial material completely from the gaps, which is not taught or suggested by Hemmenway. As previously stated, Hemmenway uses a photoresist wash to remove remaining unexposed photoresist 65 to obtain the trench-patterned structure as shown in FIG. 8 (Column 3, line 68-Column 4, line 4). Consequently, Hemmenway does not teach plasma etching sacrificial material completely from the gaps nor does Bothra cure this deficiency.

iii. Bothra fails to cure the deficiencies of Hemmenway.

Bothra discloses a method for fabricating conductive contacts in a dielectric layer that overlies a semiconductor wafer. However, Bothra does not cure the deficiencies identified above, nor does the Office Action suggest that Bothra teaches the deficiencies identified above.

In summary, it is respectfully submitted that Hemmenway and Bothra, alone or in combination, fail to teach or suggest all the claim limitations of claims 1-20. Accordingly, withdrawal of this rejection is respectfully requested for the above reasons.

II. REJECTION OF CLAIMS 21-23 UNDER 35 U.S.C. § 103

Claims 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,270,265, Hemmenway et al, hereinafter referred to as Hemmenway in view of U.S. Patent No. 6,159,844, Bothra, hereinafter referred to as Bothra. Reconsideration and withdrawal of these rejections is respectfully requested for at least the following reasons.

i. Hemmenway does not teach removing a hard mask with a dry etch.

Claims 21-23 recite removing the sacrificial layer and *the hard mask with a dry etch*, which Hemmenway and Bothra, alone or in combination, fail to teach. The Office Action contends that Hemmenway teaches performing a dry etch of the sacrificial material *and the hard mask* and points to a citation (Column 4, lines 14-17) as justification. However, that citation only discloses alternate methods of removing the *buffer material overlying the hard mask* (Column 4, line 15). Thus, the alternate methods discussed by Hemmenway are limited to only the buffer material overlying the hard mask and *not* buffer material in the gaps nor the hard mask layer, itself. Hemmenway only teaches removal of the hard mask by a wet oxide etch (Column 3, lines 61-64) as opposed to a dry etch as discussed *supra*. Furthermore, claims 21-23 include a silicon layer that could be substantially damaged by the wet oxide etch taught by Hemmenway (*see* specification, page 7, lines 27-30).

ii. Bothra again fails to cure the deficiencies of Hemmenway

As discussed above, Bothra discloses a method for fabricating conductive contacts in a dielectric layer that overlies a semiconductor wafer. However, Bothra does not cure the deficiencies identified above, nor does the Office Action suggest that Bothra teaches the deficiencies identified above. The Office Action merely relies on Bothra for teaching spin coating a photoresist mask 212, which is not a sacrificial layer

nor utilized as a sacrificial layer despite being comprised of photoresist. Further, the spin coating of the photoresist mask 212 taught by Bothra does not fill in gap(s) as does claims 21-23 of Applicants' invention.

In summary, it is respectfully submitted that Hemmenway and Bothra, alone or in combination, fail to teach or suggest all the claim limitations of claims 1-20. Accordingly, withdrawal of this rejection is respectfully requested for the above reasons.

III. NEW CLAIMS 24-26

Claims 24-26 recite removing the sacrificial layer and the hard mask with a single etch process which is not taught or suggested by the art of record. Hemmenway utilizes separate removal processes for the mask layer 11 (wet etch) and the buffer material 51 (selective irradiation and a photoresist wash) and not a singular plasma etch process to remove a sacrificial layer and a hard mask, as recited in claims 24-26. Claim 25 further recites substantially completely removing the portion of the portion of the sacrificial layer filling the gap along with the portion of the sacrificial layer covering the hard mask and the hard mask layer which is not taught or suggested by the art of record. Hemmenway requires a photoresist wash that is impervious to the underlying oxide layer to remove the remaining unexposed photoresist 65 in gaps and obtain the structure shown in FIG. 8 (Column 3, line 68-Column 4, line 4). Claim 26 recites that the single etch process is a plasma etch, which as discussed *supra*, is also not taught or suggested by the art of record.

IV. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP714US.

Respectfully submitted,
ESCHWEILER & ASSOCIATES, LLC

By _____
Thomas G. Eschweiler
Reg. No. 36,981

National City Bank Building
629 Euclid Avenue, Suite 1210
Cleveland, Ohio 44114
(216) 502-0600

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: January 9, 2003 Christine Gillroy
Christine Gillroy

T:\Amd\P714US\AMDP714US_R01.wpd

APPENDIX CONTAINING AMENDMENTS IN MARKED UP FORMAT

IN THE CLAIMS:

Please add new claims 24-26.

24. (New) A method of removing a hard mask comprising:

forming an oxide region over or within a semiconductor substrate;

forming a silicon layer over the semiconductor substrate, wherein the polysilicon layer covers the oxide region;

forming and patterning a hard mask layer over the polysilicon layer;

etching a gap in the silicon layer to expose a portion of the oxide region using the patterned hard mask as an etch mask;

forming a sacrificial layer having a relatively planar top surface over the semiconductor substrate, the sacrificial layer comprising a portion covering the hard mask layer and a portion filling the gap; and

removing the sacrificial layer and the hard mask layer with a single etch process, wherein an etch rate of the sacrificial layer and an etch rate of the hard mask layer are selected to substantially completely remove the portion of the sacrificial layer covering the hard mask and the hard mask layer, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

25. (New) The method of claim 24, wherein removing the sacrificial layer and the hard mask layer with a single etch process further comprises substantially completely removing the portion of the portion of the sacrificial layer filling the gap along with the portion of the sacrificial layer covering the hard mask and the hard mask layer.

26. (New) The method of claim 25, wherein the single etch process is a plasma etch process.